

UCD30xx Errata

Literature Number: xxxxxx

Date: January 2010

#	Description	Details	Effect	Work Around	Status
1	Switch Capacitor Timing Synchronization	Startup Timing has to be adjusted once from Power-Up	InCorrect EADC Data Values	Provided Initialization Firmware Routine	REQUIRED
2	16 bit Timer - toggling output pin as GPIO	Timer expiration event takes precedent over a GPIO write event by the CPU firmware.	If coincident events, missed GPIO data value change in Register and thus at the pin.	Write twice to the FPIO data bit within the 16 bit timer module, if timer is used internally.	
3	CLA muxing to a Master DPWM	Master DPWM can not accept output from slave CLAs, ignores CLA channel select setting	May limit Isolated DPWM configurations	Limits device pin flexibility	
4	3.3 V Ibias Drive	Delay in 3.3 Voltage Trim setting being set from default setting. Delay from Boot ROM execution of trim routine.	External pass device drive current high at initial power-up. 3.3V pin can be at 3.8 Volts for a 1ms.	None required. Within absolute maximum voltage of Device.	
5	DPWM Hi-Resolution/Montonicity	Highest setting of 250 ps edge placement can have 2 phases that are non-montonic	Jitter across two phases of Hi Resolution.	Use the 8 phaseHi-Resolution setting in the DPWMs for 500ps of accuracy.	
6	ADC12 measuring of EAP/EAN values through internal device multiplexing	Adds capacitance and load to EADC sampling	Noisy or less accurate measurement by EADC during ADC12 sampling	Use external pin connection or calculate absolute value by EADC/DAC summation	
7	PMBUS - Alert Response Message Arbitration	Im-proper arbitration on the PMBus slave when it is driving the device address, with respect to the master response of an Alert Response	Device assumes it wins arbitration on alert response.	Asserting and De-asserting of ALERT by the host can reduce the collision and need for arbitration. Configure system where the alert line is driven by only one slave.	
8	PMBUS Master Mode - Clock Stretching	Device does not support clock stretching when configured as a Master PMBUS controller	Miscommunication between slave and master devices	Cannot support clock stretched slave devices	

9	CPU Clock Divide Setting with Flash	Flash read failures when reading with divided CPU clock rates.	Corrupt Flash Reads		Reviewing Silicon process and Test coverage- Implementing Margin Read tests to cull out devices at ATE
10	PMBUS - Clock Low Timeout may force Data line to be stuck low	If Clock Low timeout coincides with a data acknowledgement by slave during a Write message, data line remains driven low even after PMBus slave resets due to Clock Low Timeout	PMBus data line stuck low	Need to perform a peripheral reset to reset all peripherals and clear PMBus slave signals	
11	Fault-2A pin	In the 40 pin package, the Fault-2A pin cannot be used as an output in Mode =000 (JTAG)	Fault -2A pin always driven as a low logic level for Mode =000	Use one of the other I/O modes, as IOMUXCTRL =111, or use just as an input for this pin.	

Note: In 40-pin package, FAULT-2A can not be used as an output when the I/O mux is set to JTAG "000". There is a bug in the I/O mux code that always drives FAULT-2A low in this configuration.